178. (Twice Amended) The method of claim 176 wherein the binary value is representative of a number of clock cycles of the external clock signal to transpire before the memory device samples the data, and wherein the first portion of the data is provided to the memory device after the number of clock cycles transpire.

Kindly **ADD** the following claims:

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198. (New) A synchronous memory device including an array of memory cells, wherein the memory device comprises:

3   a programmable register to store a binary value;

4   a plurality of input receivers to sample first and second

5   operation codes synchronously with respect to an external clock

6   signal, wherein:

7   the first operation code initiates storage of the binary

8   value in the programmable register; and

9   the second operation code initiates a read operation; and

10   a plurality of output drivers to output data in response to

11   the second operation code, wherein:

12   a first portion of the data is output synchronously with

13   respect to a rising edge transition of the external clock

14   signal; and

15   a second portion of the data is output synchronously with

16   respect to a falling edge transition of the external clock

17   signal.

1   199. (New) The memory device of claim 198 wherein the first

2   operation code is sampled synchronously with respect to a first

3   transition of the external clock signal and the second operation

4   code is sampled synchronously with respect to a second transition

5   of the external clock signal.

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1   200.   (New) The memory device of claim 199 wherein the first

2   operation code is included in a control register access packet and

3   the second operation code is included in a read request packet.

1   201. (New)   The memory device of claim 200 wherein the read

2   request packet includes address information.

1   202. (New) The memory device of claim 198 wherein the array of

2   memory cells includes dynamic memory cells.

1   203. (New) The memory device of claim 202 wherein the memory

2   device further includes a delay lock loop, coupled to the plurality

3   of output drivers, to synchronize the outputting of data with the

4   external clock signal.

1   204. (New) The memory device of claim 203 wherein the delay

2   lock loop further includes:

3   a delay line to generate an internal clock signal, wherein the

4   internal clock signal has a delay with respect to the external

5   clock signal; and

6   a comparator to compare the internal clock signal with the

7   external clock signal, wherein the delay of the internal clock

8   signal is adjusted based on the comparison between the internal

9   clock signal and the external clock signal.

1   205. (New) The memory device of claim 198 wherein the second

2   operation code includes precharge information.

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1   206. (New) The memory device of claim 205 further including a

2 plurality of sense amplifiers to access the data from the array of

3 memory cells, wherein the precharge information initiates automatic

4 precharge of the plurality of sense amplifiers after the data is

5 accessed from the array of memory cells.

1   207. (New) The memory device of claim 198 wherein the binary

2 value represents a device identifier.

1   208. (New) The memory device of claim 198 wherein the binary

2 value represents a location of a defective portion of the array of

3 memory cells.

1   209. (New) The memory device of claim 198 wherein the binary

2 value represents a delay time.

1   210. (New) The memory device of claim 198 wherein the first

2 portion of data is output, in response to the second operation

3 code, after the delay time transpires.

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